PROFI INTERFACE

LOW PRIORITY VERSION

Version 129 – 6.11.2011
http://velesoft.speccy.cz/profi.htm

This manual is for low priority firmware (pin NEW_A15 is not connect to ZX bus and memory on external devices is always enabled with higher priority). This version is usable with external MB02 interface or any DMA interface.

Configuration ports

Select ZX models:

This port set ZX mode with possibility use up to 1024kB ram. ZX PROFI,PENTAGON and SCORPION is russian ZX clones.

WRITE to port #00EF (239 dec)
READ from port #80FD (33021 dec)
D0-D1 = 2 bit value for select ZX mode:
0 = ZX 128 kB
1 = ZX PROFI 1024 kB
2 = PENTAGON 1024 kB
3 = SCORPION 1024 kB

ZX 128 mode is compatible with original ZX128/+2. Use same ports adressation, original bug in memory paging(after IN #7FFD is writed data bus value to paging port). Screen raining is enabled.

Port #7FFD adressation: A15=0 + A1=0
Port #7FFD layout:
D0 = memory bank 0
D1 = memory bank 1
D2 = memory bank 2
D3 = videoram
D4 = rom
D5 = disable port #7FFD
D6 = unused
D7 = unused

AY ports adressation: A15=1,A14=x,A1=0

ZX PROFI 1024 mode is compatible with ZX128/+2 nad russian clone ZX PROFI with 1024 kB memory. Extra memory paging on ports #7FFD and #DFFD.

Port #7FFD adressation and layout is 100% compatible with ZX 128 mode.

Port #DFFD adressation: full 16bit
Port #DFFD layout:
D0 = memory bank 3 (256 kB)
D1 = memory bank 4 (512 kB)
D2 = memory bank 5 (1024 kB)
D3 = unused
D4 = unused
D5 = unused
D6 = unused
D7 = unused
This port select 128kB block from 1MB memory.

Example: set ram page 30 in 48 basic:
OUT 57341,3 (128kB block 3 = 3x 8 pages = 24)
OUT 32765,16+6 (page 6 + 24 = page 30)

AY ports adressation: A15=1,A14=x,A13=1,A1=0

PENTAGON 1024 mode is compatible with russian clone PENTAGON 1024SL 2.2 with 1024 kB memory. Extra memory paging on port #7FFD and #EFF7.

Port #EFF7 adressation: full 16bit
Port #EFF7 layout:
D0-D1 = unused
D2 = DISABLE 1MB – 0=1MB mode/1=128kB mode
D3-D7 = unused

Port #7FFD adressation: A15=0 + A14=1 + A1=0
(same as on ZX 128+2A/+3)
Port #7FFD layout in 128kB mode is 100% compatible with ZX 128 mode.

Port #7FFD layout in 1MB mode:
D0 = memory bank 0
D1 = memory bank 1
D2 = memory bank 2
D3 = videoram
D4 = rom
D5 = memory bank 5 (compatible Pentagon 1024 kB)
D6 = memory bank 3 (compatible Pentagon 256 kB)
D7 = memory bank 4 (compatible Pentagon 512 kB)
Bits D5-D7 select 128kB block from 1MB memory.

Example: set ram page 30 in 48 basic:
OUT 32765,16+64+128+6
(+64+128=set 128kB block 3, +3=page 6)
(block 3 = 3x 8pages = 24 + page 6 = page 30)

If is set MB02 memory emulation then PENTAGON memory is limited to 512kB only and access to high 512kB ram is disabled. Second 512kB of ZX ram is used for MB02 ram and this is hardware protection of contended ram.

AY ports adressation: A15=1,A14=x,A1=0

SCORPION 1024 mode is compatible with ZX128/+2 nad russian clone SCORPION with 1024 kB memory. Extra memory paging on ports #7FFD and #1FFD.

Port #7FFD adressation: A15=0 + A14=1 + low adress A7-A0 = #FD.
Port #7FFD layout is 100% compatible with ZX 128 mode.

Port #1FFD adressation: full 16bit
Port #1FFD layout:
D0 = unused
D1 = unused
D2 = unused
D3 = unused
D4 = memory bank 3 (256 kB)
D5 = unused
D6 = memory bank 4 (512 kB)
D7 = memory bank 5 (1024 kB)
Bits D4,D6 and D7 select 128kB block from 1MB memory.

Example: set ram page 30 in 48 basic:
OUT 8189,16+64 (128kB block 3 = 3x 8 pages = 24)
OUT 32765,16+6 (page 6 + 24 = page 30)

AY ports adressation: A15=1,A14=x,A7-A0=#FD

Scorpion mode use on paging ports and AY ports full 8 bit adressation of low 8 adress lines (A0-A7). This feature enable connect external floppy drives Didaktik 40 or Didaktik 80 if you replace 64kB Scorpion rom with 4x original 48rom. D40/D80 is originally designed only for 48kB ZX models, but here can be used with 128kB ram paging (or 1MB)

Select ROM:

Select active 64kB rom from 512kB flash eprom. Each 64kB rom contain:
  128 rom
+ 48 rom
+ service monitor
+ trdos rom

WRITE to port #02EF (751   dec)
READ from port #82FD (33533 dec)
D0-D2 = 3 bit value for select 64kB block 0-7 (8x 64kB = 512kB)

Each 64kB block is used in low 16kB ZX memory as ZX rom. Bit D4 on port #7FFD select between 128 editor and 48 basic. This two roms is at begin of each 64kB block. In second two rom pages is SERVICE MONITOR (GLUK RESET SERVICE) and TR-DOS rom. GLUK rom is connect after RESET only if TRDOS is enabled. TR-DOS rom is automatically connect if TR-DOS is enabled on „interface port" and CPU jump in 48 rom to adress #3D00-#3DFF. Trdos rom is disconnect if:
1)CPU read instruction from ZX ram (#4000-#FFFF)
2)if TR-DOS is disabled on „interface port"

PROFI INTERFACE contain 512kB FLASH EPROM chip AM29F040B. After start ZX is connect always 64kB block 0. Next blocks can be connect manually. ROM 512 kB is also used in MB02 mode as rom page 0-31 with possibility enable write to rom (reflashing).

ROM blocks in 512kB flash eprom chip:

ROM BLOCK 0 = pages 0-3
ROM BLOCK 1 = pages 4-7
ROM BLOCK 2 = pages 8-11
ROM BLOCK 3 = pages 12-15

ROM BLOCK 4 = pages 16-19
ROM BLOCK 5 = pages 20-23
ROM BLOCK 6 = pages 24-27
ROM BLOCK 7 = pages 28-31

ROM EMULATION IN RAM WITH WRITE PROTECT

See details about active rom emulation on port „FEATURES". All 8 blocks ROM 64kB can be emulated in ram pages with write protect. 1MB memory in PROFI INTERFACE is divided to 16kB pages 0-63.

This is positions of emulated 64kB ROM blocks in 1MB ZX ram memory:

// blocks in first 512kB ZX ram
ROM BLOCK 0 = pages 8-11
ROM BLOCK 1 = pages 12-15
ROM BLOCK 2 = pages 16-19
ROM BLOCK 3 = pages 20-23

// blocks in second 512kB ZX ram
ROM BLOCK 4 = pages 40-43
ROM BLOCK 5 = pages 44-47
ROM BLOCK 6 = pages 48-51
ROM BLOCK 7 = pages 52-55

Example:
OUT 1007,2 (active rom emulation)
OUT 751,1 (set rom in ram 12-15)
......
OUT 1007,0 (disable rom emulation)

Same memory layout is used for DIVIDE interface (first 8kB of first page on each block is reserved for DIVIDE system, second 8kB on all 4 pages on each block is used as DIVIDE 8kB ram pages).

If any internal interface is enabled in PROFI then ROM emulation for ZX rom (rom of interface is disconnect, in low 16kB is ZX rom) is limited only to ROM BLOCK 0-3 (bit D2 of SELECT ROM port is ignored). It's limited in modes DIVIDE,TRDOS,MB02.

Interface port:

Select internal interface (memory of each interface is contended with 1MB ram and 512kB rom. After power-on or press button BUT1+RESET is always active mode 0 = external device only.

WRITE to port #01EF (495 dec)
READ from port #81FD (33277 dec)
D0-D1 = 2 bit value for select interface

0 = none
1 = DivIDE (full 100% emulation)
2 = MB02
3 = TR-DOS

- Zero value disable all interfaces.
- DivIDE mode work as original DivIDE interface, 100% compatible. DivIDE memory is: 8x (8kB rom + 32kB ram)
- MB02 mode is compatible with MB02+ memory. SRAM is full 512kB and ROM also 512kB.
- TR-DOS mode enable trdos rom maping

MODE 0 – none

All emulated interfaces is disabled.

MODE 1 – DivIDE

This mode is compatible with original(external) DivIDE interface. IDE ports support is not implemented, only DivIDE memory is used.

After active this mode is used one 64kB block of 1MB ZX ram memory as DivIDE rom + ram pages 0-3. Is possible select virtual divide 0-7 (memory layout is same as in emulation mode on ROM port). First 8kB of first page on each block is reserved for DIVIDE system, second 8kB on all 4 pages on each block is used as DIVIDE 8kB ram pages

EXAMPLE OF LAYOUT OF DIVIDE 0:
Divide ROM is at adress 0-8191 in ZX ram page 8
Divide ram 0 is in second 8kB in ZX ram page 8
Divide ram 1 is in second 8kB in ZX ram page 9
Divide ram 2 is in second 8kB in ZX ram page 10
Divide ram 3 is in second 8kB in ZX ram page 11

In DivIDE mode is enable port #E3(227 dec). This port use full 8 bit adressation and is readable on port adress #84FD(34045 dec)-return last writed value (full 8 bit data).

Port #E3 (227 dec) layout:

D0 = divide ram bank 0 (original 32kB paging)
D1 = divide ram bank 1 (original 32kB paging)
D2 = unused
D3 = unused
D4 = unused
D5 = unused
D6 = divide MAPRAM (original MAPRAM)
D7 = divide CONMEM (original CONMEM)
Extra port #17 (23 dec) is used in DIVIDE mode for select virtual divide 0-7 and next configurations. Data writed to port #17 are parallel writed also to port #E3.

Port #17 (23 dec) layout:

D0 = divide ram bank 0 (identical with port 227)
D1 = divide ram bank 1 (identical with port 227)
D2 = DBANK2 \
D3 = DBANK3 - select virtual divide 0-7
D4 = DBANK4 / (this bit select 512kB ram chips)
D5 = JUMPER – log.1 = enable writing to 8kB rom
D6 = divide MAPRAM (identical with port 227)
D7 = divide CONMEM (identical with port 227)

If CPU jump to adress #0, #8, #38, #66, #4C6, #562 then divide automatically connect at next adress in rom area 8kB divide rom + 8 kB divide ram (rom=0-8191 and ram=8192-16383). Rom is read only and ram is rewritable. Divide memory is disconnect if CPU jump to adress range #1FF8-#1FFF.(read only one instruction code from divide rom in this adress and at next adress disconnect divide memory + connect back ZX rom).
DivIDE support also trdos memory maping. Automatically connect memory if CPU jump to adress range #3D00-#3DFF. Return is same (#1FF8-#1FFF).

More information about DivIDE interface:
http://velesoft.speccy.cz/zx/divide/doc/pgm_model-en.txt
Original system flashers for DivIDE interface work on PROFI INTERFACE correct, but must be enable writing to divide rom (bit JUMPER of port 23 must be set to log.1). If write protect is active, then will system install to mapram mode only. Bits DBANK 2-4 select virtual divide 0-7
D0-D1 on port #E3 select divide 8kB ram 0-3
Each DivIDE ram page is contended with 1MB memory and use only last 8kB of each 16kB ZX ram page.
Bit D7 (CONMEM) of port #E3 is used for static connect divide memory in low 16kB (ignore DivIDE memory maping, CONMEM use higher priority). CONMEM also enable writing to low 8kB divide rom if JUMPER=1 on port #17. After install system must be set JUMPER to log.0)
Example:

```
LD A,8
OUT (23),A (select virtual divide 2)
LD A,128
OUT (227),A (disable ZX rom and connect divide rom with write protect + divide ram 0)

LD A,64+3
OUT (227),A (switch divide to MAPRAM mode with layout ram3 with write protect + ram3 with write protect)

LD A,32
OUT (23),A (set JUMPER=1 – write enable rom)
LD A,128
OUT (227),A (disable ZX ROM and connect divide rom with write enable + divide ram 0)
```

Systems as FATWARE, ESXDOS, MDOS3, DEMFIR, +DIVIDE, GASWARE, DIVIDE BIOS and T-BIOS work on PROFI INTERFACE correct. DivIDE allram mode are not implemented (ignored). BS-DOS 309 and RESIDOS work in MB02 mode... PROFI INTERFACE use memory without IDE ports, then must be connect to your ZX also IDE interface,MB IDE or DIVIDE for possibility use all this systems.

Divide memory layout in 1MB ram

```
// blocks in first 512kB ZX ram
DIVIDE 0 = pages  8-11
DIVIDE 1 = pages 12-15
DIVIDE 2 = pages 16-19
DIVIDE 3 = pages 20-23

// blocks in second 512kB ZX ram
DIVIDE 4 = pages 40-43
DIVIDE 5 = pages 44-47
DIVIDE 6 = pages 48-51
DIVIDE 7 = pages 52-55
```

MODE 2 - MB02:

Compatible mode with MB02+ interface (only memory paging is used from MB02+).

After active this mode will active value on port #17 (this port is enabled also out of MB02 mode). After write correct value to MB02 paging port will in low 16kB connect MB02 memory ram or rom page with 16kB size.

Second 512kB of 1MB memory is used for full 512kB MB02 ram. All 512kB flash eprom in PROFI is used as 512kB MB02 rom.

```
MB02 ram 0 is in ZX ram page 32
MB02 ram 1 is in ZX ram page 33
MB02 ram 2 is in ZX ram page 34
MB02 ram 3 is in ZX ram page 35
...
MB02 ram 31 is in ZX ram page 63

MB02 ROM 0-31 is in FLASH EPROM 512kB page 0-31
```

In MB02 mode is enable port #17(23 dec). This port use full 8 bit adressation and is readable from port #84FD(34045 dec) !!! IN #84FD return real value of MB02 port (full 8 bit data).

Port #17 (23 dec) layout:

```
D0 = MB02 ram bank 0
D1 = MB02 ram bank 1
D2 = MB02 ram bank 2
D3 = MB02 ram bank 3
D4 = MB02 ram bank 4

D5 = WRITE ENABLE (0=read only / 1=write enable)

D6 = MB02 RAM enable (0=disable/1=enable ram)
D7 = MB02 ROM enable (0=disable/1=enable rom)
```

Possible combinations:

```
D6=0 + D7=0 = ZX rom
D6=1 + D7=0 = MB02 ram page
D6=0 + D7=1 = MB02 rom page
D6=1 + D7=1 = ZX rom
```

Example:

```
LD A,128+5
OUT (#17),A (disable ZX rom and connect MB02 rom
page 5 with write protect)

LD A,128+32+2
OUT (#17),A (disable ZX rom and connect MB02 rom
page 2 with write enable)

LD A,64+1
OUT (#17),A (disable ZX rom and connect MB02 ram
page 1 with write protect)

LD A,64+6+32
OUT (#17),A (disable ZX rom and connect MB02 ram
page 6 with write enable)

LD A,31
OUT (#17),A (enable ZX rom + only write value to
port #17 = without effect)

LD A,128+64+32
OUT (#17),A (enable ZX rom + only write value to
port #17 = without effect)
```

After press BUT1 button CPU only jump to adress 102 (original MB02 after NMI jump to page 0 with write protect). But after press external NMI (on ZX bus) set page 0 with write protect + CPU jump to adress #66 as on original MB02+. RESET only jump to adress 0 in actual MB02 page.

PROFI INTERFACE use MB02 memory without IDE ports, then must be connect to your ZX also IDE interface,MB IDE or DIVIDE for possibility use MB02 systems as BS-DOS 309 or RESIDOS.

(After connect external interface UR-4 to ZX BUS is possible install also MB02 versions of systems FATWARE and DEMFIR. This systems use register backup to chip 8255)

MODE 3 – TR-DOS:

This mode use TR-DOS rom maping as on BETA-DISC interface/russian ZX clones.

After active this mode is TR-DOS rom disconnect. Only if CPU jump in 48 rom (if D4=1 on port #7FFD) to adress range #3D00-#3DFF then will automatically connect TR-DOS rom (last 16kB of active 64kB rom block). TR-DOS rom will disconnect if CPU jump to ZX ram (out of rom). (in active trdos rom is possible switch between GLUK rom and TRDOS rom via set bit D4 of port 7FFD – 0=GLUK/1=TRDOS)

Original old TR-DOS rom versions 5.03 or Czech 5.05 is unusable – real FDD absent !!!
(If you connect to ZX bus interface with WD1793 controller, then is possible use real FDD and compatibility with real BETA-DISC will 100%). Actually PROFI INTERFACE can use higher versions of TR-DOS with ramdisc support in 1MB memory. Ramdisc is TRD image in ZX ram and size can be different (512kB, full 640kB, 768kB or 896kB). On different TR-DOS versions is ramdisc connect to different drive (A-D). TR-DOS for ZX PROFI 1024 use ramdisc on drive D, TR-DOS for PENTAGON 1024 use ramdisc on drive D or A(my patched TR-DOS version). RAMDISC on all trdos versions is compatible with software/games using standard trdos services only (call #3D13).

After reset in TRDOS mode will always connect GLUK monitor(rom 2) with comfortable menu. External NMI(on ZX bus) is always enabled and BUT1 button(internal NMI button on PROFI interface) is disabled in TRDOS mode. TRDOS rom is part of 64kB ROM block and can be also emulated in ZX ram (see ROM PORT for details)

Features port:

Port for set new features.

WRITE to port #03EF (1007 dec)
READ from port #83FD (33789 dec)

D0 = turbo/fast mode
(1=fast ports and memory)

D1 = ROMEMUL
(1=rom emulation in protected ZX ram)

TURBO/FAST MODE:
Disable contention adress of ports and memory. All ports with A0=1 is fast as on ZX128+2A/+3/ZX clones. All memory 1MB is fast, only first 8kB(8192 bytes) on memory pages 5 and 7 is slow(contended) as on original ZX128.
If turbo is OFF then ports and memory contention is identical with original ZX128.

ROMEMUL:
Log.1 active ROM emulation in ZX ram.
See ROM PORT details...

Memory port:

READ ONLY port – return true number of memory page in high 16kB, state of videoram and rom type.

READ from port #85FD (34301 dec)

D0 = ZX memory bank 0
D1 = ZX memory bank 1
D2 = ZX memory bank 2

D3 = ZX memory bank 3
D4 = ZX memory bank 4
D5 = ZX memory bank 5

D6 = active VIDEORAM (0 or 1)

D7 = ROM bit (0=128 editor/1=48 basic)

BANK0-BANK2 sign D0-D2 from port #7FFD

Bits BANK3-BANK5 sign next paging bits from additional paging ports for 1MB memory.

After press RESET button is all paging ports (#7FFD,#EFF7,#DFFD,#1FFD) reset, is set 128 editor (or GLUK rom if TRDOS is enable)and CPU jump to adress 0.

Status port:

READ ONLY port – return status of internal registers in PROFI INTERFACE.

READ from port #86FD (33557 dec)

D0 = DIS128 - bit D5 of port 7FFD
(sign if port 7FFD is disabled)

D1 = EFF7_D2 – bit D2 of port EFF7
(0=1MB or 1=128kB in Pentagon mode)

D2 = TRDOS
(0=in low 16kB is ZX rom/1= TR-DOS rom)

D3 = DIV_MAP
(0=in low 16kB is ZX rom/1= divide memory – no sign CONMEM)

D4 = PRESS_RESET
(0=state without reset/1=state after reset button)

D5 = NMI button state
(1=active)

D6 = BUT1 button state
(1=active)

Clear RESET port:

WRITE ONLY port – after write any value to this port is reset value of bit D4 on status port(PRESS_RESET).

WRITE to port #04EF (1263 dec)

D0-D7 is ignored, any value can be writed to this port

Detect port:

READ ONLY port – return version of firmware for PROFI INTERFACE. This firmware use value #80 (128 dec)

READ from port #87FD (34813 dec)

D0–D7 = 8 bit value

Additional info about PROFI:

PROFI INTERFACE automatically set IM 2 vector on data bus to #FF(255 dec) via pull-up resistors.